InfoVision Optoelectronics (Kunshan) Co.,LTD.

Document Title	P190MWW1 Product Information			Page No.	1/27
Document No.		Issue date	2009/03/23	Revision	00

IVO Product Information

To:

Product Name: P190MWW1

-404

Document Issue Date: 2009/03/23

Customer	InfoVision Optoelectronics
SIGNATURE	**SIGNATURE**
	QA
	PREPARED BY
	FAE
Please return 1 copy for your confirmation with your signature and comments.	

Note: 1. Please contact InfoVision Company. Before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

FQ-7-30-0-009-03D

NO.1 Long Teng Road, KunShan City, JiangSu, China
InfoVision Optoelectronics (Kunshan) Co., LTD
Tel:0512-57278888
Fax:0512-57278900

Revision	Date	Page	Old Description	New Description	Remark
00	2009/03/23	all	--	First issued.	-

Contents

1.0 GENERAL DESCRIPTIONS

1.1 Introduction

The **P190MWW1** is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controler, voltage reference, common voltage, driver DC-DC converter, column driver, and row driver circuit. This TFT LCD has a 19-inch diagonally measured active display area with WXGA+ resolution (1440 vertical by 900 horizontal pixel array).

1.2 Features

- 19”WXGA+ TFT LCD Panel
- 4 CCFLs Backlight System
- Supported WXGA+ (V:1440 lines, H:900 pixels) resolution
- Supported to 75Hz Refresh Rate
- Compatible with RoHS Standard

1.3 Product Summary

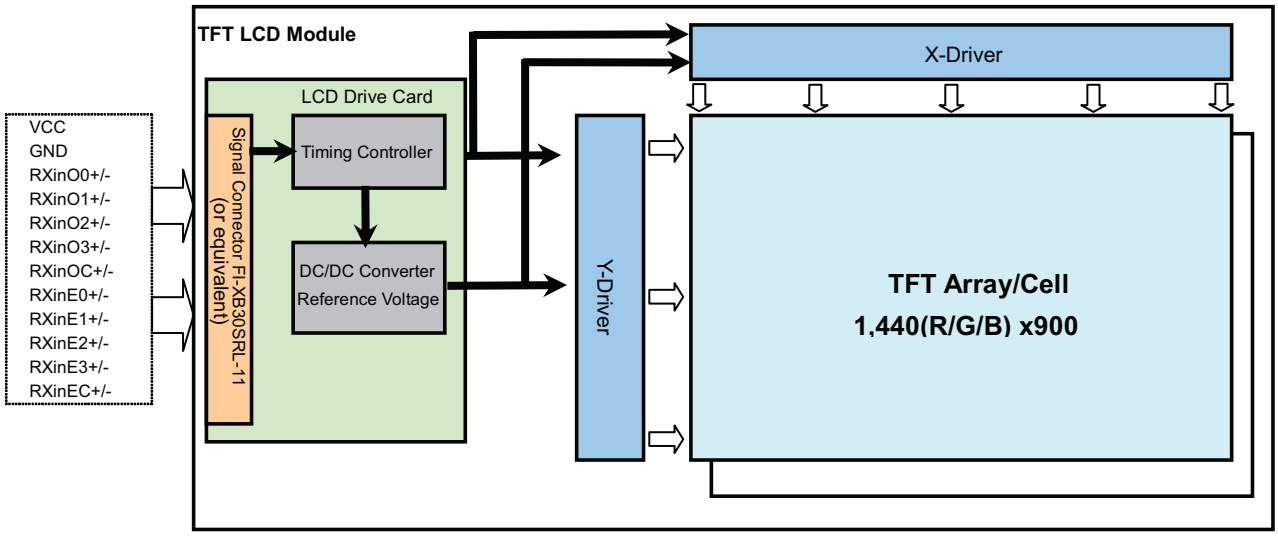
Items	Specifications	Unit
Screen Diagonal	19.05 inch	Inch
Active Area	410.4(H) x 256.5(V)	mm
Pixels H x V	1,440 (x3) x 900	
Pixel Pitch	0.285 (per one triad) x 0.285	mm
Pixel Arrangement	R.G.B. Vertical Stripe	
Display Mode	Normally White	
Contrast Ratio	1000 : 1 typical	
Color Saturation	72%	NTSC
Response Time	5 typical	msec
Input Voltage	+ 5.0 typical	V
Logic Power Consumption	2.6 typical (Black pattern, 60Hz)	Watt
Electrical Interface (Logic)	6bit+Hi-FRC dual LVDS	
Support Color	16.7M	
Optimum Viewing Direction	6 o’clock	
Surface Treatment	Anti Glare + HC	

1.4 Functional Block Diagram

.

Figure 1 shows the functional block diagram of the LCD module.

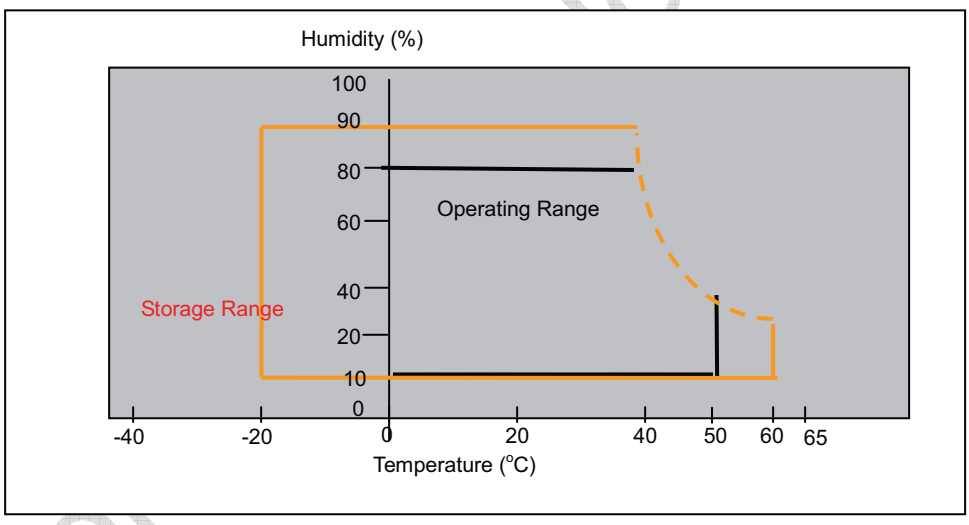
Figure 1 Block Diagram



2.0 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+6.0	V	
Input Signal		-0.3	+2.7	V	LVDS signals
Operating Temperature	TOP	0	+50	Deg. C	(Note)
Operating Humidity	HOP	10	80	%RH	(Note)
Storage Temperature	TST	-20	+60	Deg. C	(Note)
Storage Humidity	HST	10	90	%RH	(Note)

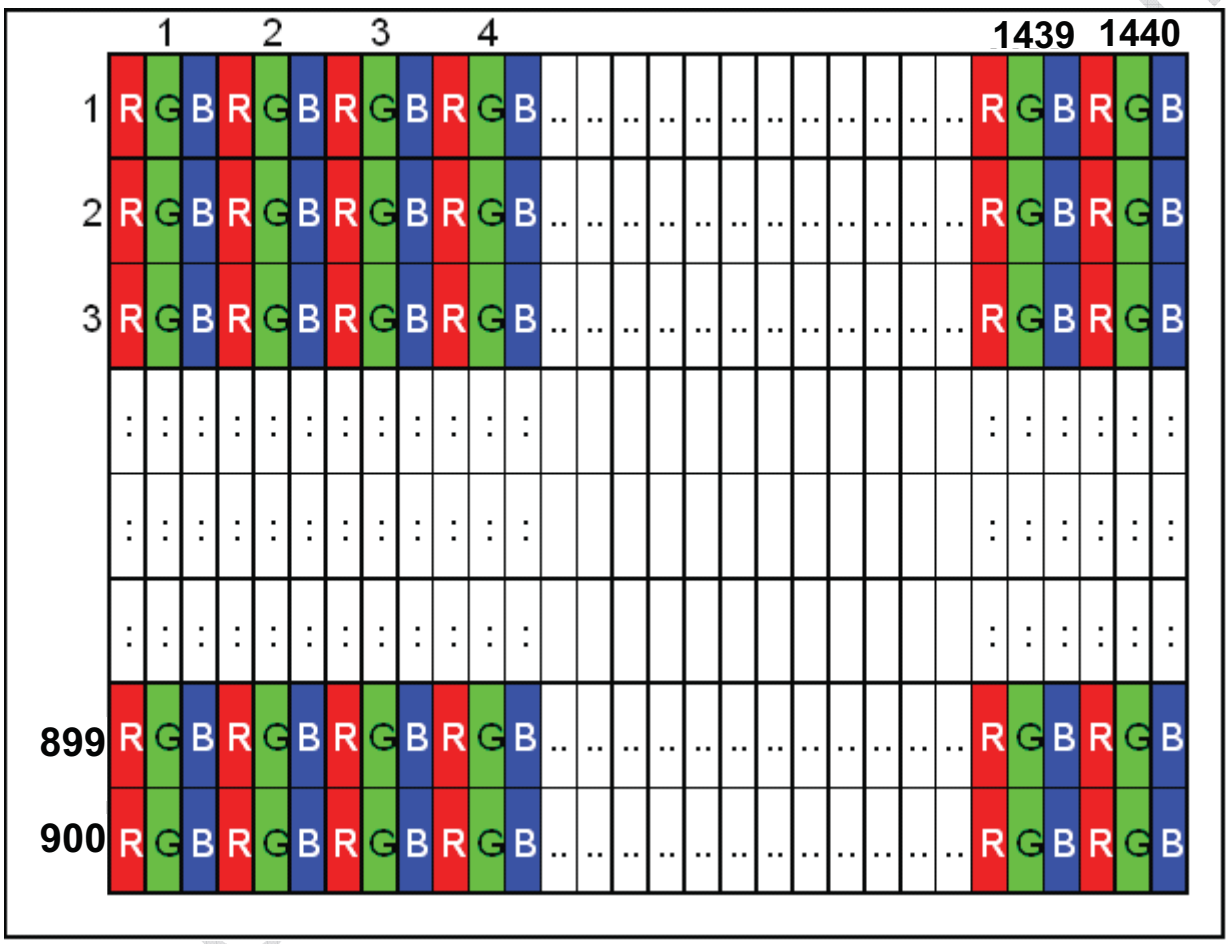
Note(1) Storage /Operating temperature. Maximum Wet-Bulb should be 39 degree C.
No condensation.



3.0 Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

Table 1 Optical characteristics

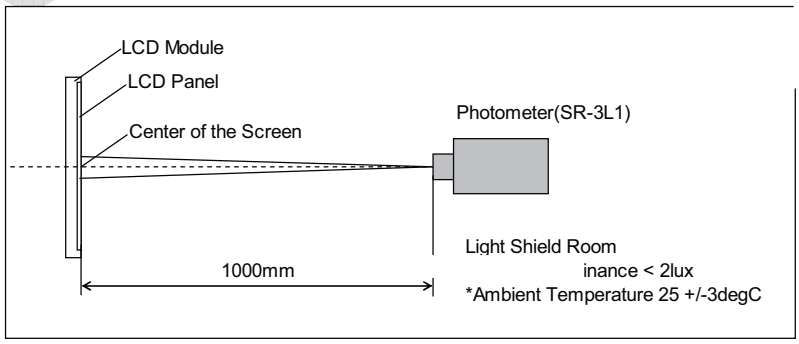
Item	Conditions	Specification			
		Min	Typ.	Max	Note
Viewing Angle [degrees]	Horizontal (Right + Left)	140	160	--	A, B
K=Contrast Ratio>10	Vertical (Up + Down)	140	160	--	
Contrast ratio		750	1000	--	A, C
Response Time [ms]	Rising + Falling	--	5	10	A, D
Color Chromaticity	Red x	0.621	0.651	0.681	A,
(CIE1931)	Red y	0.307	0.337	0.367	A,
	Green x	0.255	0.285	0.315	A,
	Green y	0.580	0.610	0.640	A,
	Blue x	0.113	0.143	0.173	A,
	Blue y	0.039	0.069	0.099	A,
	White x	0.283	0.313	0.343	A,
	White y	0.299	0.329	0.359	A,
Panel Transmittance (%)		4.71	5.23		

Note:

A. Measurement Setup:

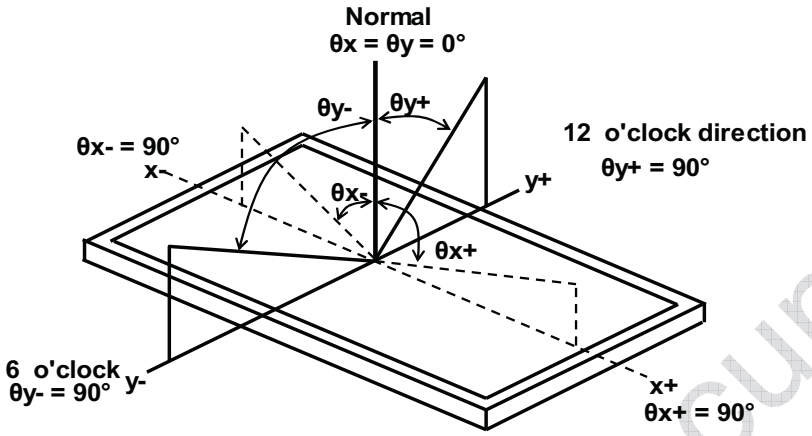
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes in a windless room.

Figure 3 Measurement Setup



B. Definition of Viewing Angle

Figure 4 Definition of Viewing Angle



C. Definition of Contrast Ratio (CR)

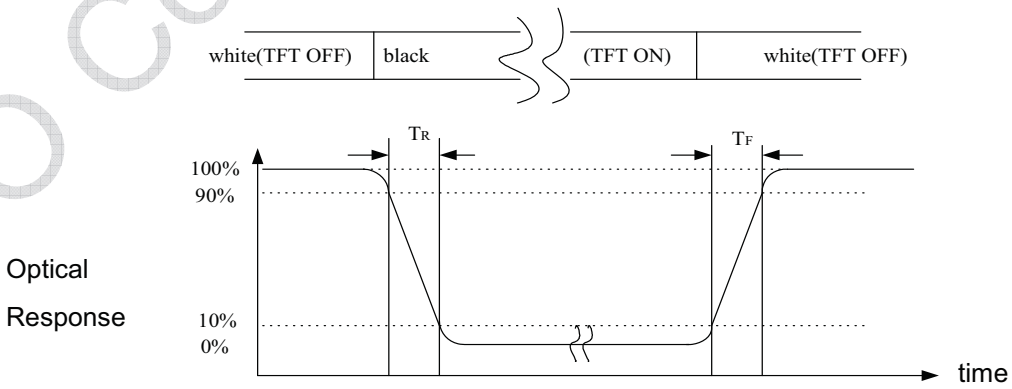
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

D. Definition of Response Time (T_R, T_F)

Figure 5 Definition of Response Time



E. Definition of Luminance White

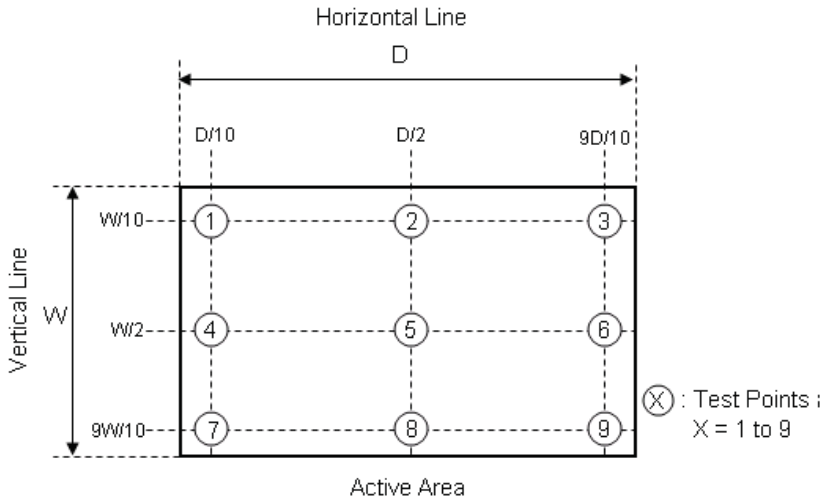
Measure the luminance of gray level 255 at center point

F. Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 255 at 9 points.

$$\mathrm{UNF(9pts)} = \frac{\max(L1, L2, \cdots L9)}{\min(L1, L2, \cdots L9)}$$

Figure 6 Measurement Locations of 9 Points



5.0 Electrical Characteristics

5.1 Interface Connector

Table 2 Connector Name / Designation

Manufacturer	JAE (or equivalent)
Type / Part Number	UJU IS100-L30R-C23(A)
Mating Receptacle/Part Number	JAE FI-X30H(L), JAE FI-X30C*(L), JAE FI-X30M*

Table 3 Signal pin assignment

Pin #	Signal Name	Description	Remarks
1	RXinO0-	LVDS differential data input	
2	RXinO0+	LVDS differential data input	
3	RXinO1-	LVDS differential data input	
4	RXinO1+	LVDS differential data input	
5	RXinO2-	LVDS differential data input	
6	RXinO2+	LVDS differential data input	
7	GND	Ground	
8	RXOC-	LVDS differential data input	
9	RXOC+	LVDS differential data input	
10	RXinO3-	LVDS differential data input	
11	RXinO3+	LVDS differential data input	
12	RXinE0-	LVDS differential data input	
13	RXinE0+	LVDS differential data input	
14	GND	Ground	
15	RXinE1-	LVDS differential data input	
16	RXinE1+	LVDS differential data input	
17	GND	Ground	
18	RXinE2-	LVDS differential data input	
19	RXinE2+	LVDS differential data input	
20	RXEC-	LVDS differential data input	
21	RXEC+	LVDS differential data input	
22	RXinE3-	LVDS differential data input	
23	RXinE3+	LVDS differential data input	
24	GND	Ground	
25	GND	Ground	
26	NC	Reserved for LCD manufacturer.	

27	GND	Ground	
28	VCC	Power Supply	
29	VCC	Power Supply	
30	VCC	Power Supply	

All input signals shall be low or Hi-Z state when VDD is off.

5.2 LVDS Receiver

5.2.1 Signal Electrical Characteristics for LVDS Receiver

The built-in LVDS receiver is compatible with ANSI/TIA/TIA-644 standard.

Table 4 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth	--	--	+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100	--	--	mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	--	600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	ΔVcm	-50	--	+50	mV	Vth - Vtl = 200mV

Note:

A. Input signals shall be low or Hi-Z state when VDD is off.

B. All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Table 5 Timing Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	Note
Clock Frequency	Fc	40.8	44.5	65.0	MHz		
Input Data Skew Margin	Trskm	-850		+850	ps	Fc=44.5MHz, |Vth-Vtl| = 400mV Vcm = 1.2V, ΔVcm = 0	(Figure **11**11)

Note: All values are at VDD=5.0V, Ta=25 degree C.

Figure 8 Voltage Definitions

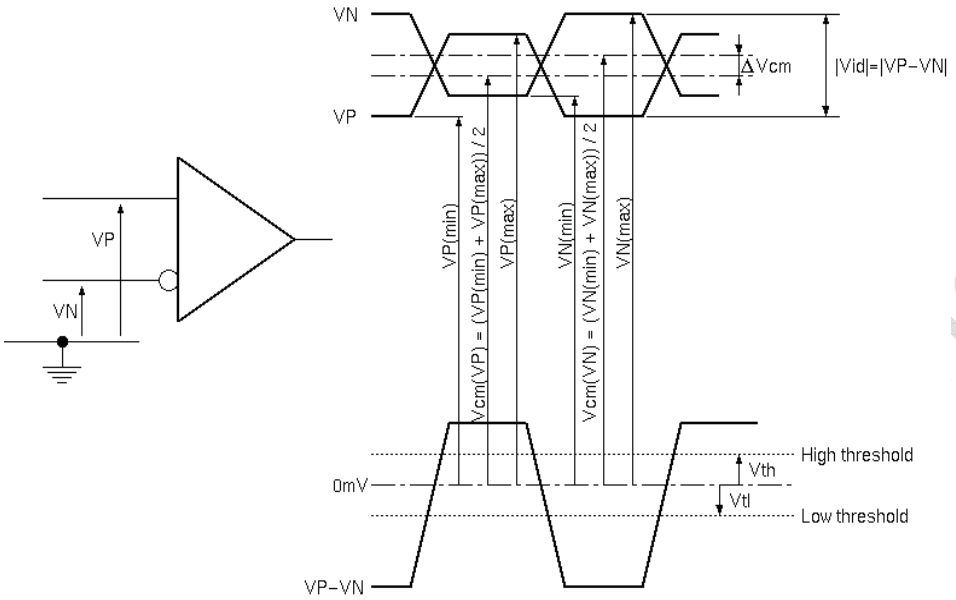


Figure 9 Measurement System

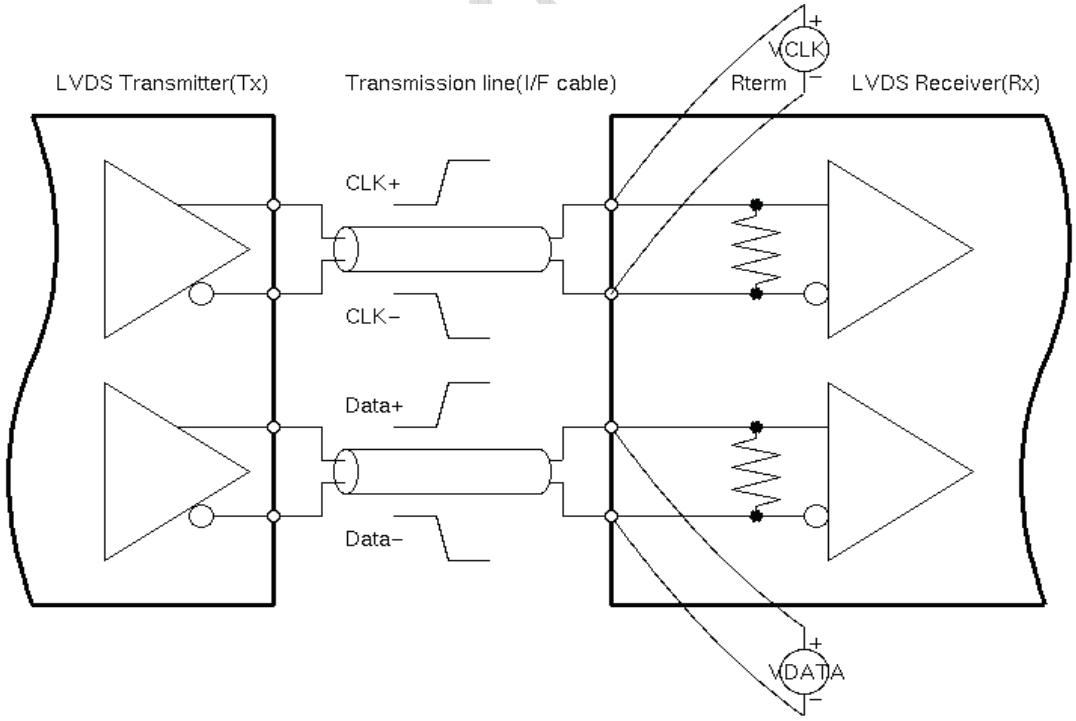


Figure 10 Data mapping

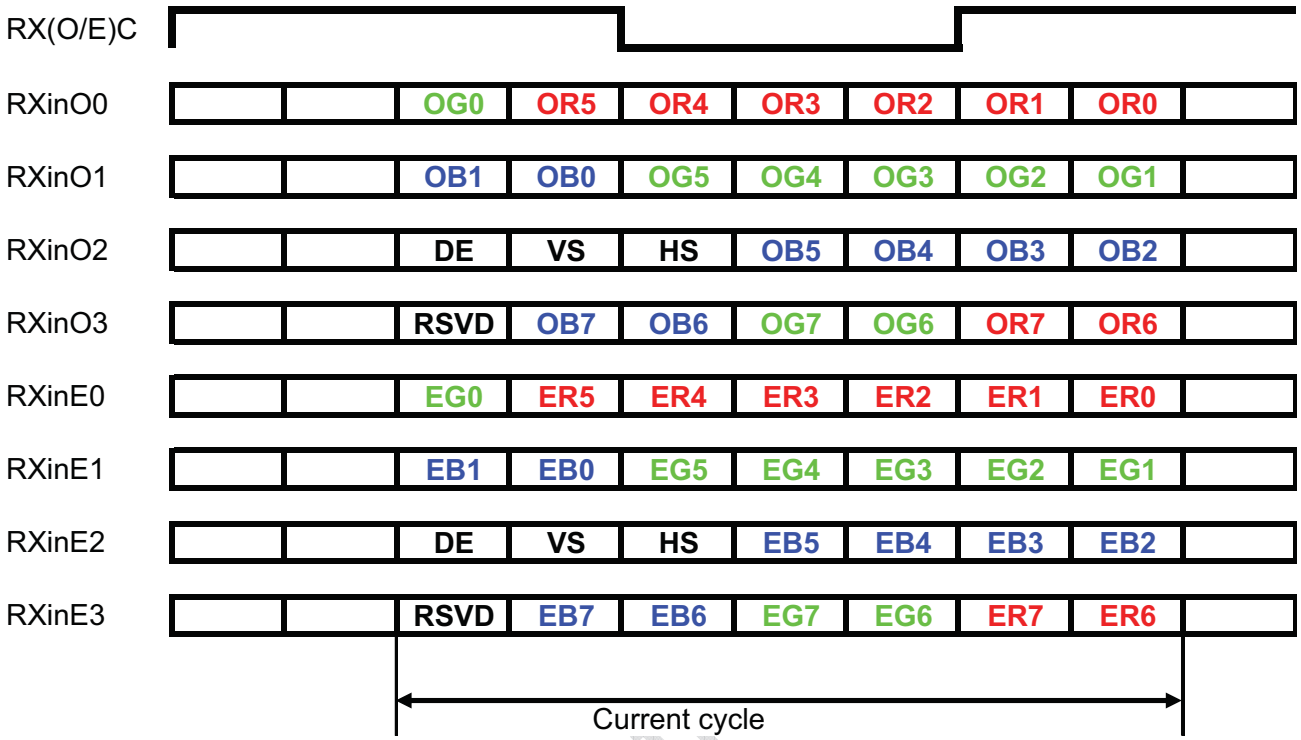
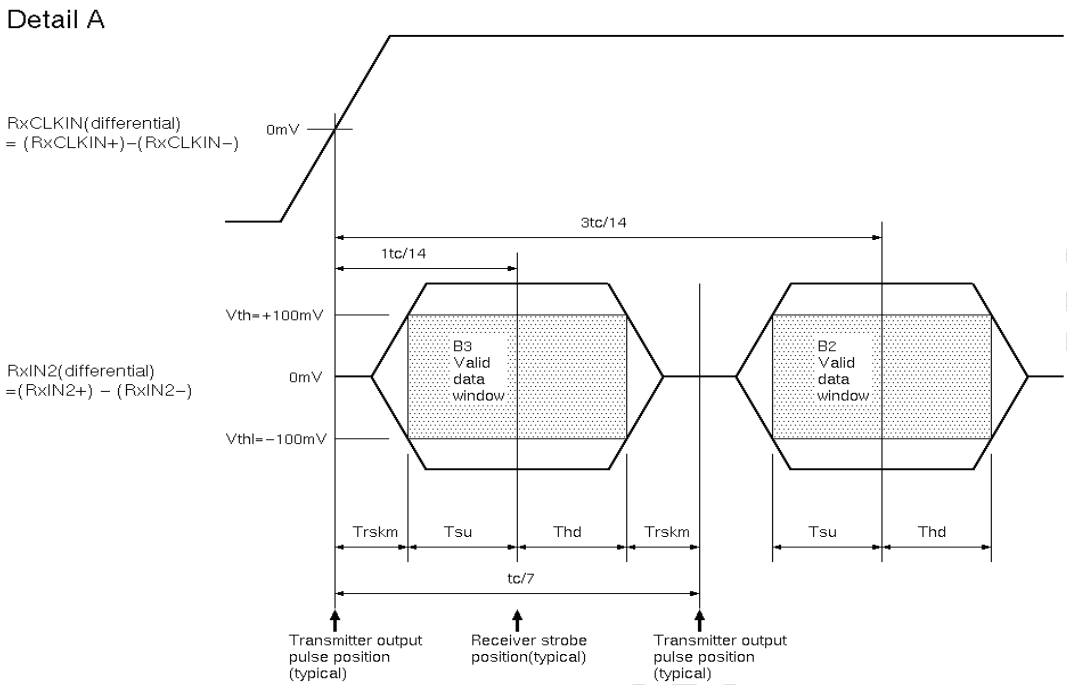


Figure 11 Timing Definition

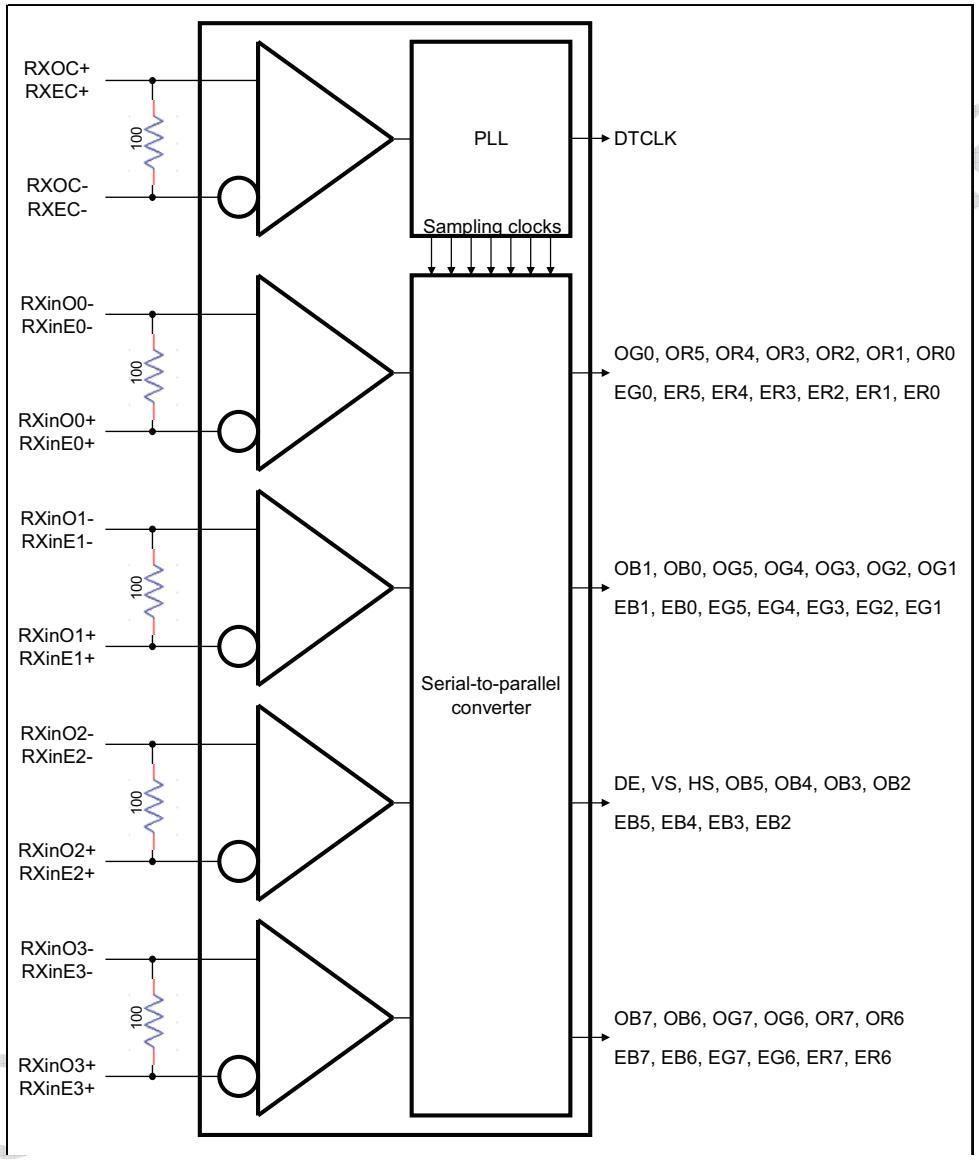


Note: Tsu and Thd is internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.2.2 LVDS Receiver Internal Circuit

Figure 12 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 12 LVDS Receiver Internal Circuit



6.0 Interface Timings

6.1 Timing Characteristics

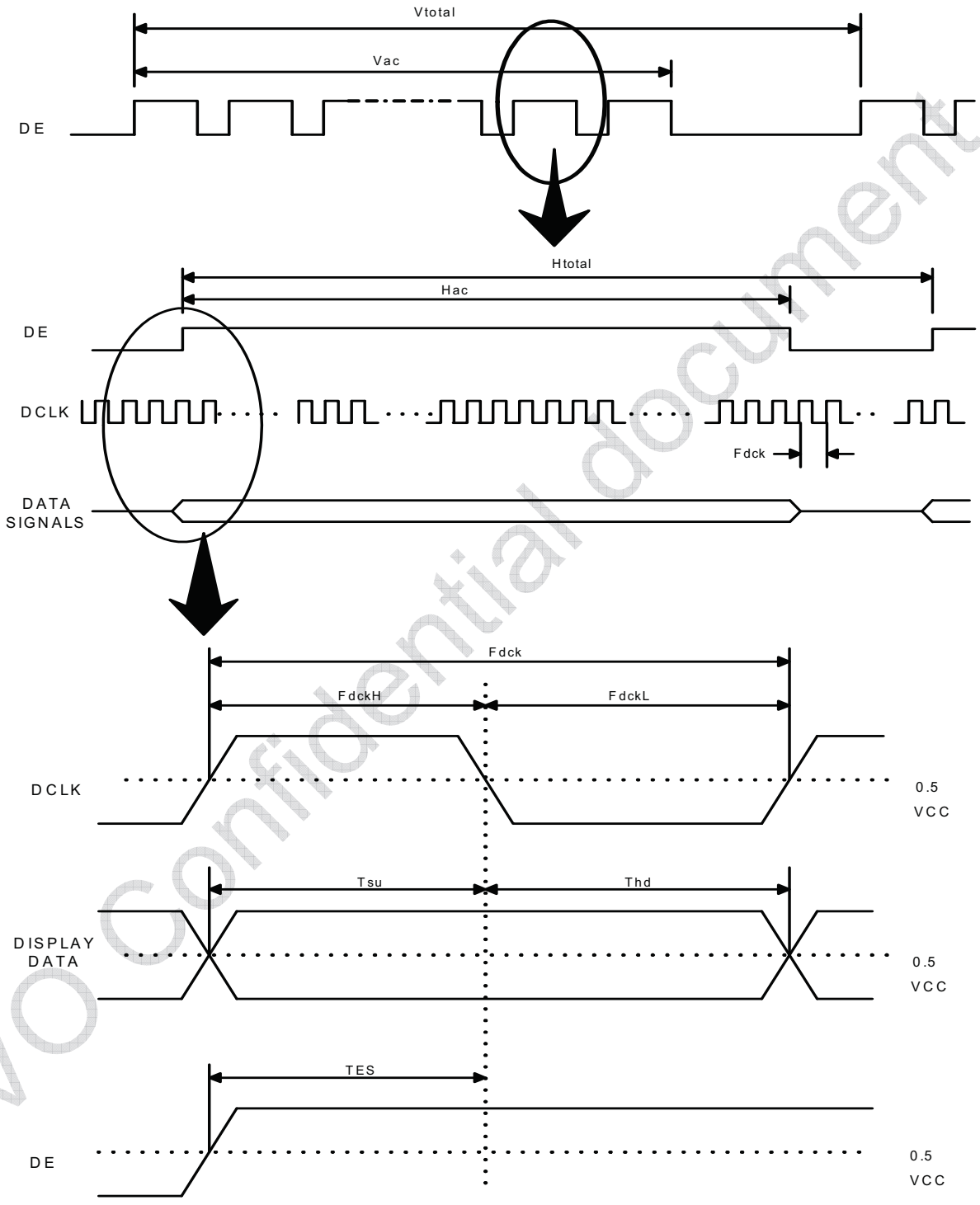
Table 6 Interface timings

Parameter	Symbol	Unit	Min	Typ	Max
LVDS Clock Frequency(dual)	Fdck	MHz	40.8	44.5	65.0
H Total Time	Htotal	clocks	760	800	1398
H Active Time	Hac	clocks	720	720	720
V Total Time	Vtotal	lines	905	926	1599
V Active Time	Vac	lines	900	900	900
Frame Rate	Vsync	Hz	55	60.0	75.0

Note (1) This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

(2) Internal Vcc= 3.3V.

Figure 13 Timing Characteristics



Note: TES is data enable signal setup time.

7.0 Power Consumption

Input power specifications are as follows.

Table 7 Power consumption

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[V]	
IDD	VDD Current	-	0.60	-	[A]	All black pattern, 60Hz
		-	-	0.95	[A]	Max pattern, 75Hz
PDD	VDD Power	-	2.5	-	[W]	All black pattern, 60Hz
		-	-	4.3	[W]	Max pattern, 75Hz
Irush	Rush Current	-	-	4.5	[A]	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	300	[mVp-p]	

8.0 Power ON/OFF sequence

VDD power, interface signals, and lamp on/off sequence are shown in Figure .Signals shall be Hi-Z state or low level when VDD is off.

Figure 14 Power sequence

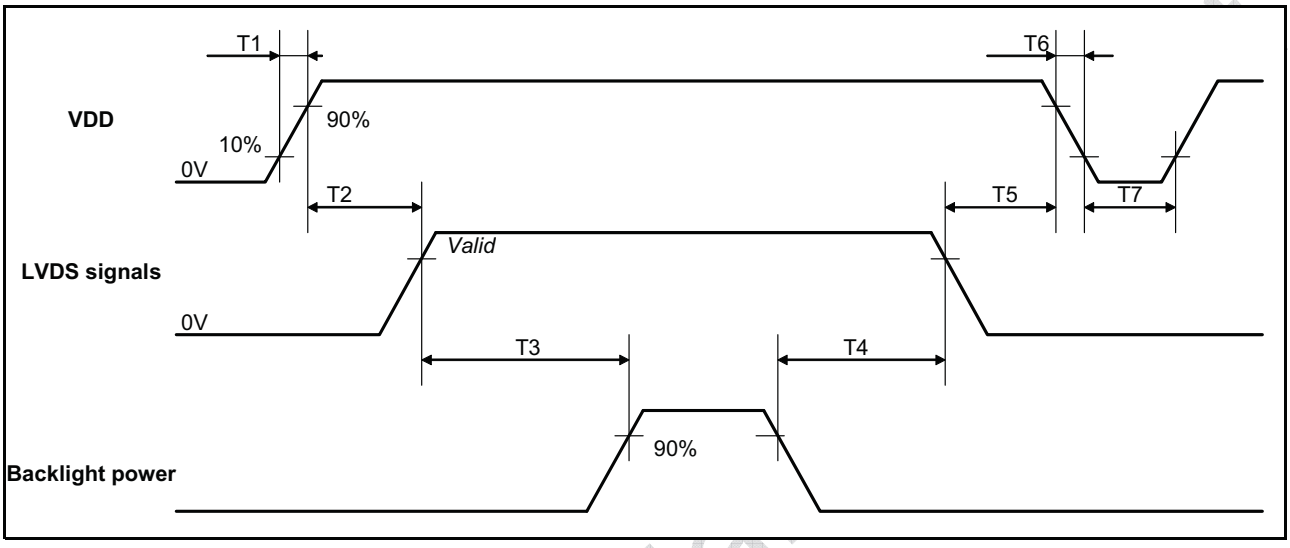
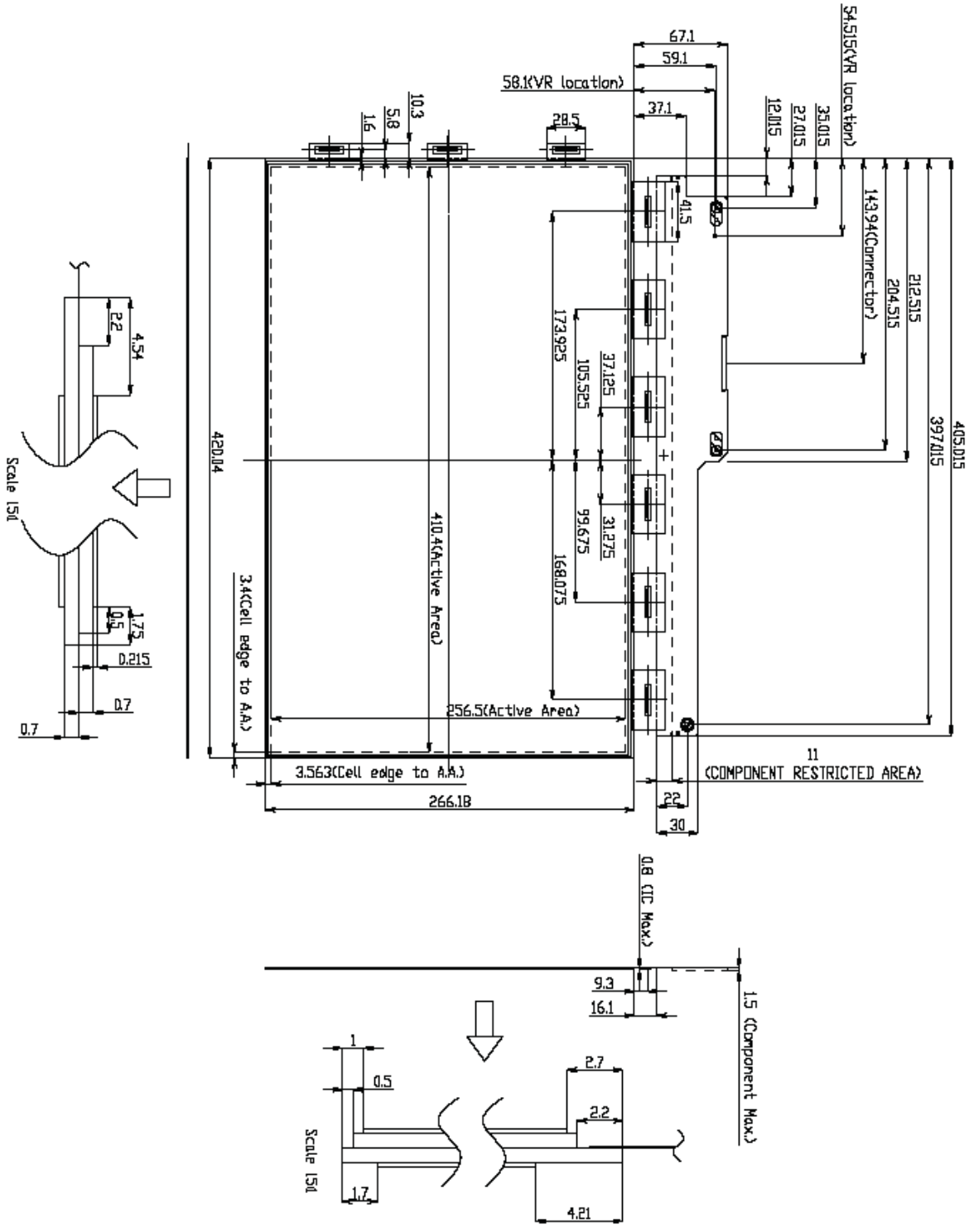


Table 8 Power Sequencing Requirements

Parameter	Symbol	Unit	Min.	Typ.	Max.
VDD Rise Time	T1	ms	0.5	-	10
VDD Good to Signal Valid	T2	ms	0	-	10
Signal Valid to Backlight On	T3	ms	200	-	-
Backlight Off to Signal Disable	T4	ms	100	-	-
Signal Disable to Power Down	T5	ms	0	-	50
VDD Fall Time	T6	ms	-	-	10
Power Off	T7	ms	1000	-	-

9.0 Mechanical Characteristics

Figure 7 Reference outline drawing (Front side)

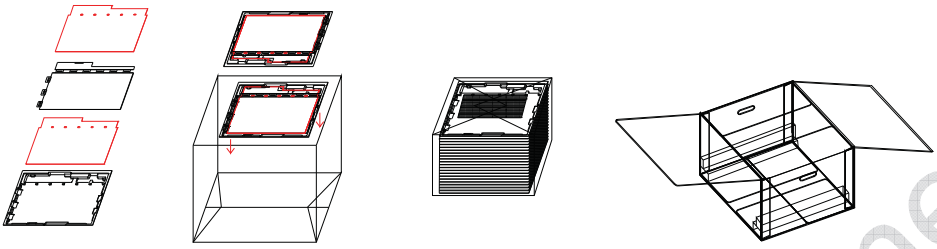


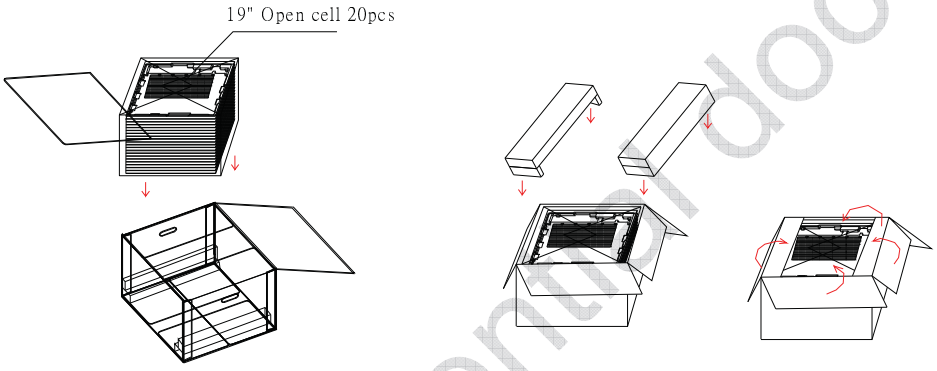
9.1 Dimension Specifications

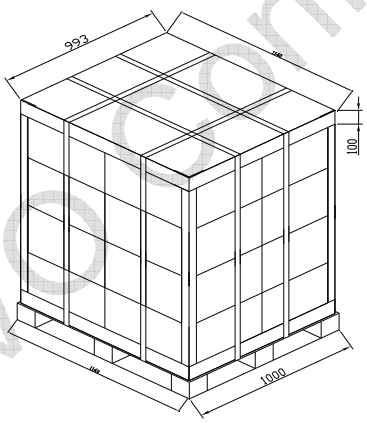
Table 9 Module Dimension Specifications

Width [mm]		333.28 ± 0.5
Height [mm]		420.04 ± 0.5
Thickness [mm]	Glass(Cell)	1.83 ± 0.21
	PCB	0.8 ± 0.1
	Component	1.5(Max)
Weight [g]		470 ±25

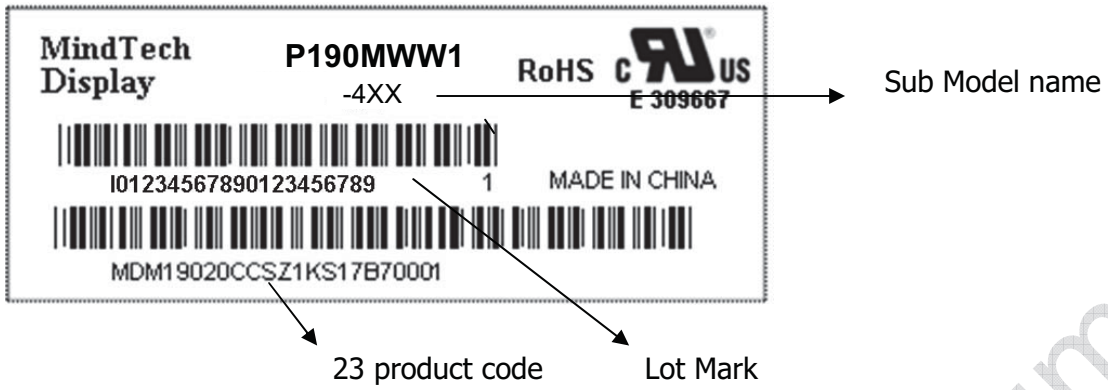
10.0 PACKAGE SPECIFICATION







11.0 LOT MARK



11.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,3,6,7,8,9,10,11: MTDis internal flow control code.
code 5: production location.
code 12: production year.
code 13: production month.
code 16,17,18,19,20: serial number.

Note (1) Production Year

Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Mark	6	7	8	9	A	B	C	D	F	G

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

11.2 23 product barcode

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: MD Mindtech Display.
code 3,4,5,6,7: MTDis internal module name.
code 8,9,10,13,16: MTDis internal flow control code.
code 11,12: Cell location Suzhou defined as “SZ”.
code 14 ,15: Module line kunshan defined as” KS”.
code 17,18,19 : Year, Month, Day Refer to MTDis barcode Note(1),Note(2).
code 20~23 : Serial Number.

12.0 GENERAL PRECAUTION

12.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

12.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. MTD does not warrant the module, if customers disassemble or modify the module.

12.3 Breakage of LCD Panel

12.3.A If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin.

12.3.B If liquid crystal contacts mouth or eyes, rinse out with water immediately.

12.3.C If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.

12.3.D Handle carefully with chips of glass that may cause injury, when the glass is Broken

12.4 Electric Shock

12.4.A Disconnect power supply before handling LCD module.

12.4.B Do not pull or fold the CCFL cable.

12.4.C Do not touch the parts inside LCD modules and the fluorescent lamp's connector Or cables in order to prevent electric shock

12.5 Absolute Maximum Ratings and Power Protection Circuit

12.5.A Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD module may be damaged.

12.5.B Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

12.5.C It's recommended employing protection circuit for power supply.

12.6 Operation

12.6.A Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.

12.6.B When the surface is dusty, please wipe gently with absorbent cotton or other soft Material

12.6.C Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading

12.6.D When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent

12.7 Mechanism

Please mount LCD module by using mounting holes arranged in four corners tightly.

12.8 Static Electricity

12.8.A Protection film must remove very slowly from the surface of LCD module to Prevent from electrostatic occurrence.

12.8.B Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge

12.8.C Persons who handle the module should be grounded through adequate methods.

12.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, Display characteristics may be changed.

12.10 Disposal

When disposing LCD module, obey the local environmental regulations.